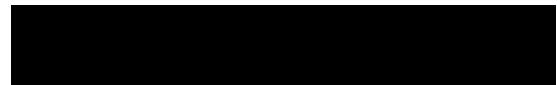


# EXHIBIT T



**Exhibit F - Infringement of U.S. Patent 9,318,160**

Netlist notes that these preliminary infringement contentions are based on publicly available information. Netlist expects that information to be revealed in future discovery may result in identification of additional instances of Micron's infringement, and may also enable identification of additional claims infringed by Micron. The claims asserted, and the theories set forth herein are based on Netlist's present understanding of the Accused Instrumentalities. Netlist reserves the right to supplement or amend these contentions as permitted by the Local Rules and any Orders of the Court as discovery progresses. Further, these contentions contain images and examples illustrating Netlist's infringement theories. As such, the images and examples are not intended, and should not be read, as narrowing or limiting the scope of these contentions. On information and belief, the examples are representative of the Accused HBM Products in material aspects.

The Accused Instrumentalities include, without limitation, any Micron high bandwidth memory ("HBM") products with 8 or more stacked DRAM dies made, sold, offered for sale, used and/or imported into the United States by Micron and any other Micron products that operate in the substantially similar manner. By way of non-limiting example, the accused HBM products include products having the following part numbers MT54A8G804000BF and MT54A16G804000AC and any HBM products that are structure and operated in materially the same way in material aspects. Information for Micron's HBM products can be found via Micron's web page, such as <https://www.micron.com/products> and <https://www.crucial.com/products>.

Micron also infringes through acts of inducement and contributory infringement.

**Exhibit F - Infringement of U.S. Patent 9,318,160**

<b>Claim 1</b>	<b>Evidence of Use</b>
<p><b>(1d)</b> a control die comprising first data conduits between the first die interconnects and the data terminals, and second data conduits between the second die interconnects and the data terminals, the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies, the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size.</p>	<p>The Accused Instrumentalities further comprise a control die comprising first data conduits between the first die interconnects and the data terminals, and second data conduits between the second die interconnects and the data terminals, the first data conduit including first drivers each having a first driver size and configured to drive a data signal from a corresponding data terminal to the first group of array dies, the second data conduit including second drivers each having a second driver size and configured to drive a data signal from a corresponding data terminal to the second group of at least one array die, the second driver size being different from the first driver size.</p> <p>The Accused Instrumentalities also include a control die, <i>e.g.</i>, at the bottom of the memory package (i.e. the “logic die,” “base die,” or “interface die”), which is vertically interconnected by TSVs and associated bumps and bond pads to the corresponding array dies.</p> <p>On information and belief, the control die further includes first data conduits between the first die interconnects and the data terminals, and second data conduits between the second die interconnects and the data terminals.</p> 